

Tachyssema HV3 MODULE User's Guide

NOTICES

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Certification

This delivered module is guaranteed ROHS and lead free.

Safety informations

While unused and packaged, the module must be stored in a proper anti static bag.

Proper grounding technique and anti static methods must be carefully used when the module is plugged in a board or device.

All power supply must be off when the module is plugged or external connections are made.

The 3.3V power supply ramp up while the module is being powered up must meet the requirements given in the Lattice ECP3 data sheet.

Disclaimer

The information contained in this guide is accurate to the best of our knowledge, but may evolve due to corrections or technical progress without notice.

Package content

Your module package must contain the following items:

- (1) HV3 module
- (1) CD with supporting documents, supporting project files, and technical examples

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1 MODULE OVERVIEW

1.a Module Description

This HV3 module is a very low profile high density FPGA module including all that is needed for a complete solution for advanced stand alone operation.

The Lattice ECP3 family is targeting high demand and flexibility which is possible due to the power of its architecture, a mix of high density fabric with a multitude of embedded resources ranging from sysDSP and sysMEM blocks to 3.125Gbps SERDES.

The Tachyssema HV3 module offers a compact solution optimized for advanced data processing and embedded applications. It includes: Two DDR2 memories, two flash memories, all power and configuration management, a clock, and more extras. A high speed connector provides the interfaces to the world in the form of SERDES ports or multi standard discrete digital signals.

The DDR2 RAM offers a large real-time flow buffering, real-time swap space capability, and a large application memory.

The embedded FLASH memories give a perfect stand-alone ability: The CFI typically stores application code and reference objects while the SPI circuit stores the FPGA configuration bit stream.

The high-speed connectivity permits the exploitation of the large FPGA flow acquisition and generation ability.

In addition, the optional implementation of the MICO32 soft core processor and the μ Clinux environment can convert the module into an embedded platform to be used as a very powerful and flexible tool. Refer to the MICO32 section and its μ Clinux port on the Lattice web site www.latticesemi.com

All the programming of the FPGA is done with the Lattice tool suite. Several examples and low level routines are provided on a CD with the module. These include examples of MICO32 systems as well as VHDL only projects.

In all, this HV3 module provides the user with an exceptional functionality along an extremely efficient architecture.

1.b Bloc Diagram

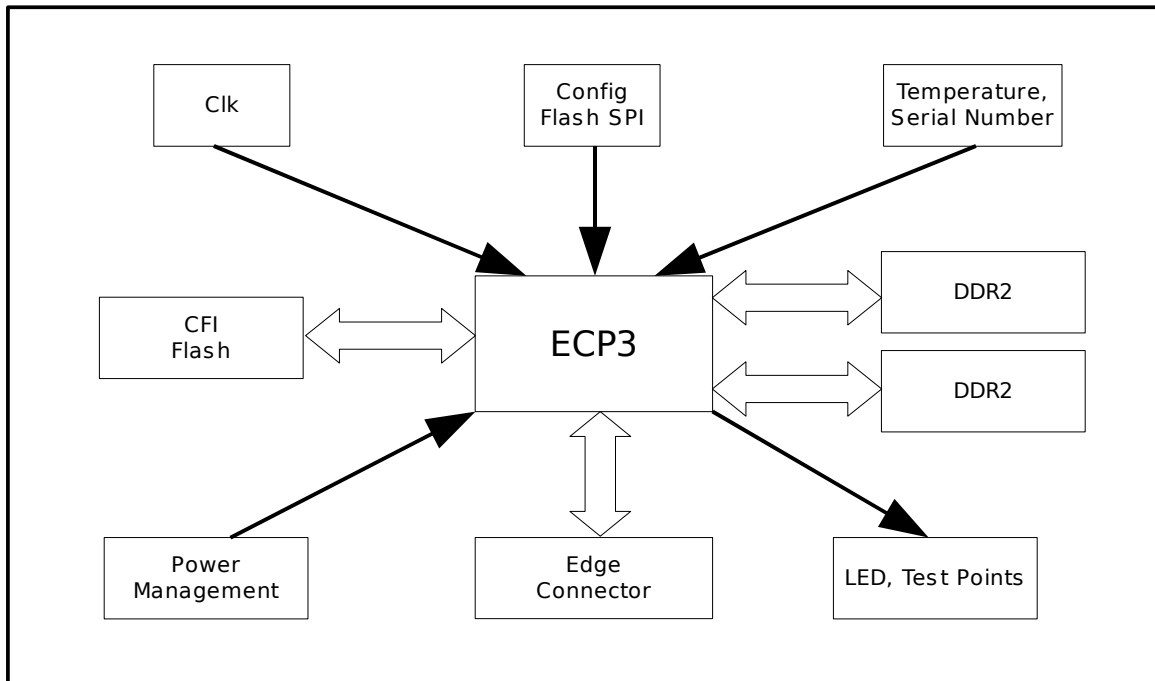


Illustration 1: Module block diagram

1.c Module Specifications

	HV3 Module
FPGA package	fpBGA 672
ECP3 density	70 / 95 / 150 (Klut 67 / 92 / 149)
DDR2	(x2) 1Gb @400MHz
CFI flash	512Mb / 1Gb
External I/Os	32
High speed links	(x8) SERDES @3.125Gb/s
Configuration	32Mb / 64Mb SPI
Oscillator and clock capabilities	High quality 125MHz local oscillator (x10) low jitter cascadable PLLs (x2) DLLs
EBR SRAM Blocks	240 / 240 / 372 (4420 / 4420 / 6850 Kbits)
18 x 18 Multipliers	128 / 128 / 320
Dimensions (mm)	59 x 62 mm
MICO 32	Optionally embedded in the device as soft core license free IP
µC-Linux	Optionally embedded in CFI flash
Supply voltage	Single 3.3V

Table 1: Module specifications

1.d Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
3R3	Power supply input	3.135	3.3	3.465	V
VIO	Banks 2/3 alternative supply	1.14	1.2 to 3.3	3.465	V
TS	Storage temperature	-50		+150	°C
TJ	FPGA junction temperature			+125	°C

Table 2: Absolute maximum ratings

1.e Module Layout

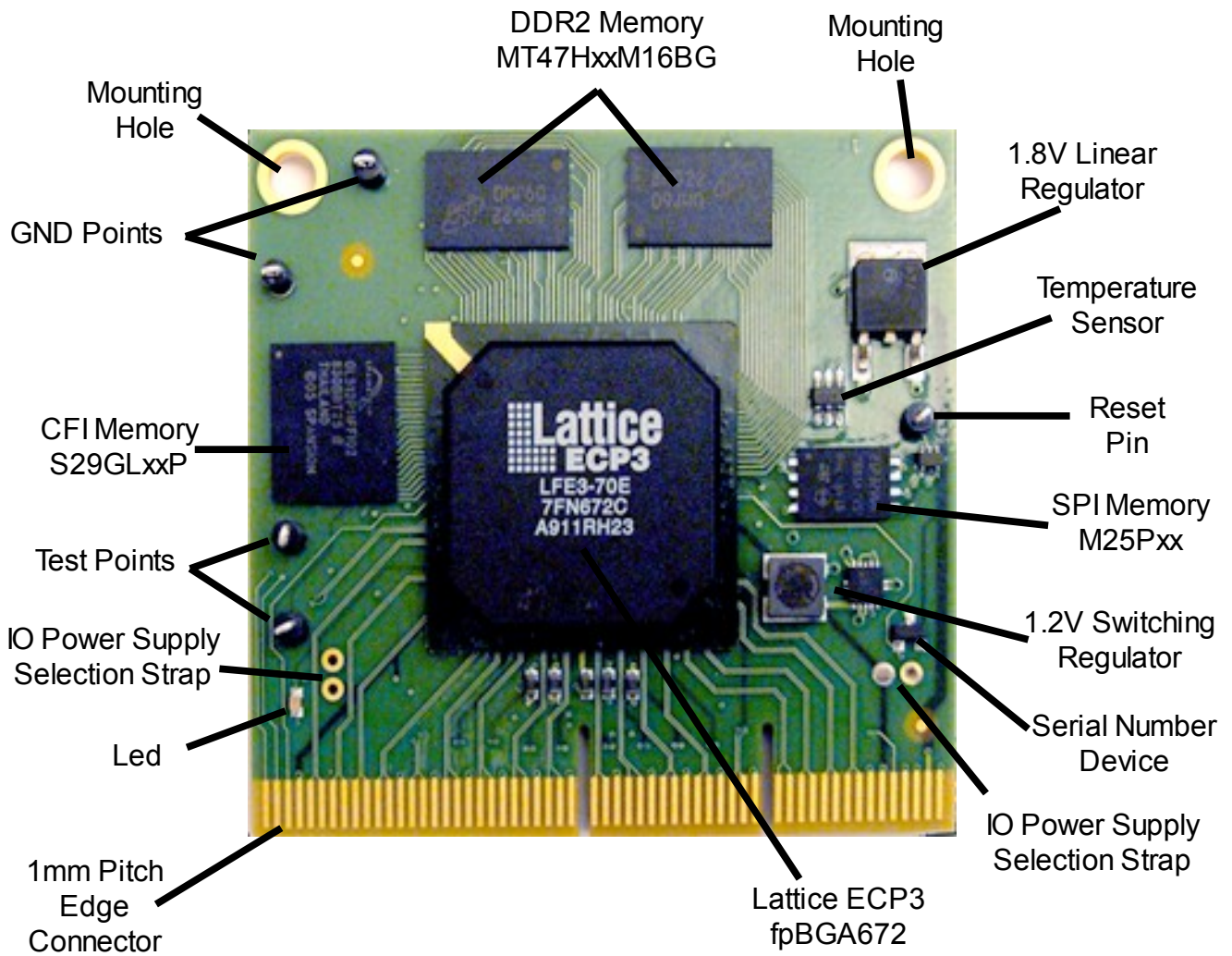


Illustration 2: HV3 Module layout

1.f Mechanical Drawing

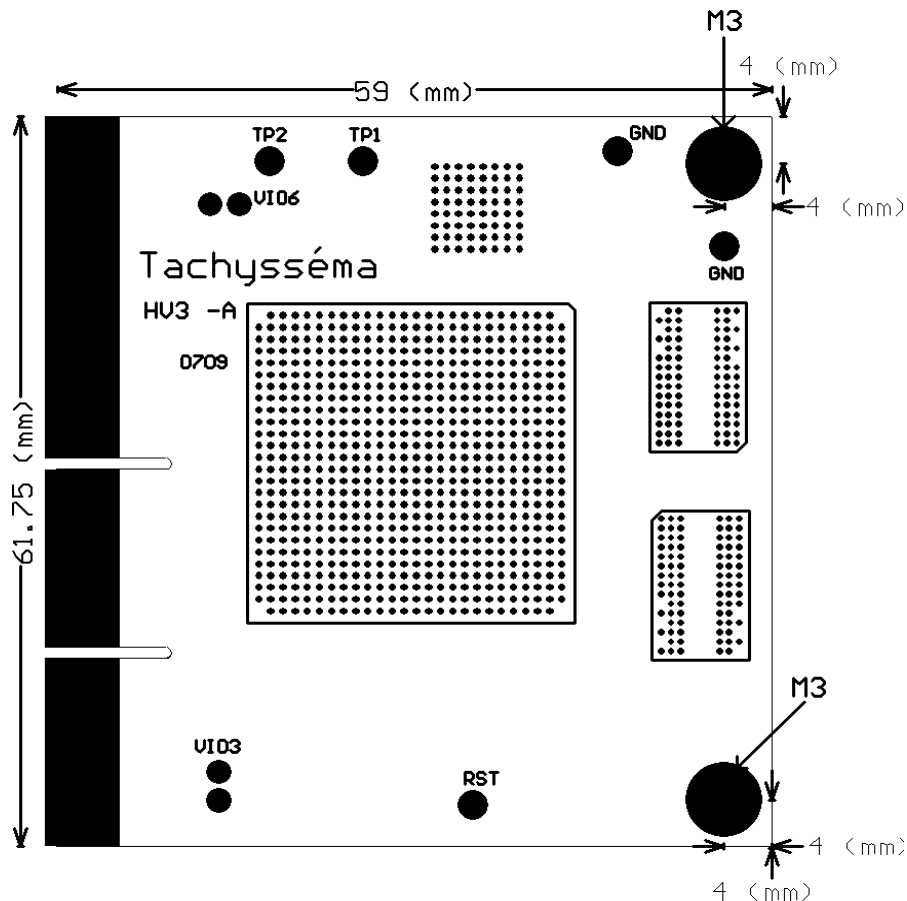


Illustration 3: Mechanical drawing, top view

The module is plugged on a motherboard via the edge connector into a Samtec receptacle. Refer to the “Edge Connector Overview” section regarding Samtec options and part numbers.

Evaluation motherboards are available for many configurations. Refer to the Tachyssema web site (www.tachyssema.com) for technical references as well as options and availability.

The module is secured to the motherboard via two M3 inserts.

Refer to the Samtec documentation regarding the implementation and specifications of the receptacle on a motherboard. Both horizontal and vertical mounting styles are available.

If mounted horizontally, a keep out area for no components should be placed on the motherboard's top side underneath the module. Only vias are allowed on the motherboard's top side there.

The module's top side profile is 5mm high. However, without the test points, it is only 3mm. It is possible to specify the module with the test points uninstalled for very low profile production requirements.

2 EXTERNAL I/Os

2.a Edge Connector Overview

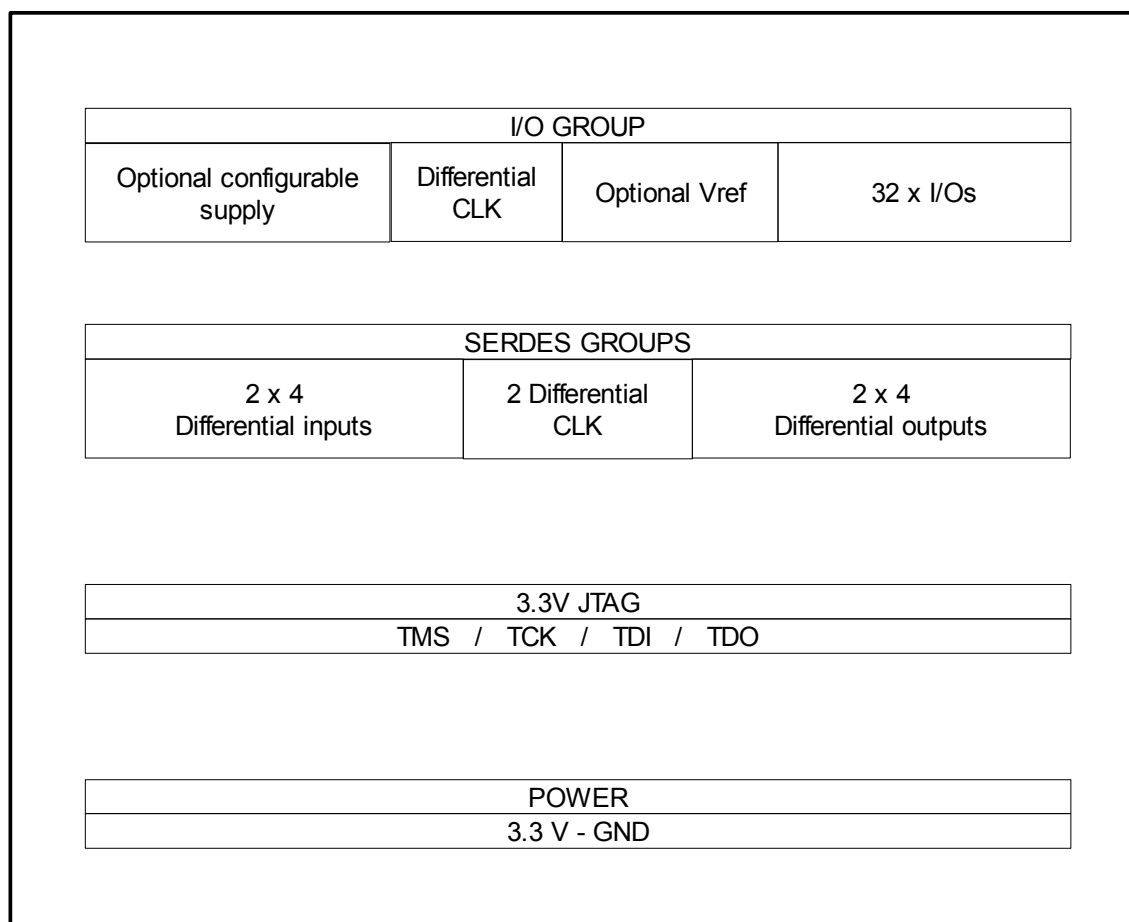


Illustration 4: Edge connector overview

The module plugs into a specific PCB receptacle. Connector possibilities include horizontal or vertical module mounting.

For horizontal mounting, use a Samtec MEC1-160-02-L-D-RA1 connector, or equivalent.

For vertical mounting, use a Samtec MEC1-160-02-L-D connector, or equivalent.

Bottom Side Signal		Edge Connector Pinout		Top Side Signal	
GND	GND	1	2	GND	GND
1R8	Power supply monitoring	3	4	Power supply monitoring	1R8
3R3	Main power supply input	5	6	Main power supply input	3R3
		7	8		
VT3	Banks03 termination voltage	9	10	Banks03 threshold reference voltage	B3REF
VIO3	Banks03 alternative supply	11	12	Banks03 alternative supply	VIO3
1R2	Power supply monitoring	13	14	Power supply monitoring	1R2
B3IO8	Banks03 I/Os	15	16	Banks03 I/Os	B3IO0
B3IO9		17	18		B3IO1
B3IO10		19	20		B3IO2
B3IO11		21	22		B3IO3
B3IO12		23	24		B3IO4
B3IO13		25	26		B3IO5
B3IO14		27	28		B3IO6
B3IO15		29	30		B3IO7
	Connector key	31	32	Connector key	
GND	GND	33	34	GND	GND
CKA1	SerDes Clock P	35	36	Bank03 differential clock	B3CKP
CKA0	SerDes Clock N	37	38		B3CKN
GND	GND	39	40	GND	GND
INA0	SerDes Input P chanel0	41	42	SerDes Output P chanel0	OUTA0
INA1	SerDes Input N chanel0	43	44	SerDes Output N chanel0	OUTA1
GND	GND	45	46	GND	GND
INA3	SerDes Input N chanel1	47	48	SerDes Output N chanel1	OUTA3
INA2	SerDes Input P chanel1	49	50	SerDes Output P chanel1	OUTA2
GND	GND	51	52	GND	GND
INA4	SerDes Input P chanel2	53	54	SerDes Output P chanel2	OUTA4
INA5	SerDes Input N chanel2	55	56	SerDes Output N chanel2	OUTA5
GND	GND	57	58	GND	GND
INA7	SerDes Input N chanel3	59	60	SerDes Output N chanel3	OUTA7
INA6	SerDes Input P chanel3	61	62	SerDes Output P chanel3	OUTA6
	Connector key	63	64	Connector key	
GND	GND	65	66	GND	GND
INB0	SerDes Input P chanel0	67	68	SerDes Output P chanel0	OUTB0
INB1	SerDes Input N chanel0	69	70	SerDes Output N chanel0	OUTB1
GND	GND	71	72	GND	GND

INB3	SerDes Input N chanel1	73	74	SerDes Output N chanel1	OUTB3
INB2	SerDes Input P chanel1	75	76	SerDes Output P chanel1	OUTB2
GND	GND	77	78	GND	GND
INB4	SerDes Input P chanel2	79	80	SerDes Output P chanel2	OUTB4
INB5	SerDes Input N chanel2	81	82	SerDes Output N chanel2	OUTB5
GND	GND	83	84	GND	GND
INB7	SerDes Input N chanel3	85	86	SerDes Output N chanel3	OUTB7
INB6	SerDes Input P chanel3	87	88	SerDes Output P chanel3	OUTB6
GND	GND	89	90	GND	GND
CKB1	SerDes Clock N	91	92	Bank06 differential clock	B6CKP
CKB0	SerDes Clock P	93	94		B6CKN
GND	GND	95	96	GND	GND
B6IO8	Banks06 I/Os	97	98	Banks06 I/Os	B6IO0
B6IO9		99	100		B6IO1
B6IO10		101	102		B6IO2
B6IO11		103	104		B6IO3
B6IO12		105	106		B6IO4
B6IO13		107	108		B6IO5
B6IO14		109	110		B6IO6
B6IO15		111	112		B6IO7
VIO6	Banks06 alternative supply	113	114	Banks06 alternative supply	VIO6
VT6	Banks06 termination voltage	115	116	Banks06 threshold reference voltage	B6REF
TCK	JTAG	117	118	JTAG	TDI
TDO		119	120		TMS

Table 3: Edge connector pin out

2.b Power Supply

The HV module is powered by a single 3.3V supply.

The other required voltages, $V_{core} = 1.2V$ and $V_{ddr} = 1.8V$, are derived on board from the 3.3V supply, using a switcher and a linear regulator respectively..

As for all FPGA based systems, the current required to operate the module depends upon the design itself, its speed, density, and peripheral used.

Nevertheless, the power estimation tool from Lattice can be used to size the external 3.3V power supply. Refer to the Lattice technical notes regarding proper air flow and thermal management techniques for if needed.

As starting point examples, several mid size applications (MICO32 + quad SERDES outputs) have been measured to draw less than 0.5A at 3.3V.

2.c SERDES Links

The two quad full-duplex SERDES I/O links and reference clocks available on the Lattice ECP3-70/95 FPGA in the fpBGA672 package are brought out to the interface connector. These are referenced as PCSA and PCSB links through the Lattice documentation.

A 100 Ω termination resistor is installed between the differential traces of the reference clocks.

Refer to the Lattice user's guides specific to the usage of the SERDES for complete specifications.

Signal	Edge Connector	FPGA	Signal	Edge Connector	FPGA
INA0	41	AD21	INB0	67	AD13
INA1	43	AD20	INB1	69	AD12
INA2	49	AD18	INB2	75	AD10
INA3	47	AD19	INB3	73	AD11
INA4	53	AD17	INB4	79	AD9
INA5	55	AD16	INB5	81	AD8
INA6	61	AD14	INB6	87	AD6
INA7	59	AD15	INB7	85	AD7
OUTA0	42	AF21	OUTB0	68	AF13
OUTA1	44	AF20	OUTB1	70	AF12
OUTA2	50	AF18	OUTB2	76	AF10
OUTA3	48	AF19	OUTB3	74	AF11
OUTA4	54	AF17	OUTB4	80	AF9
OUTA5	56	AF16	OUTB5	82	AF8
OUTA6	62	AF14	OUTB6	88	AF6
OUTA7	60	AF15	OUTB7	86	AF7
CKA0	37	AC17	CKB0	93	AC9
CKA1	35	AC18	CKB1	91	AC10

Table 4: SERDES links pin out

2.d External Clocks

Two user external clocks are available on the edge connector. They are

B3CKP/N: Bank 3, VIO=VIO3, connected to FPGA PCLK T/C.

B6CKN/P: Bank 6, VIO=VIO6, connected to FPGA PCLK T/C.

Refer to the Lattice user's guide related to clocks and clock management system for further information, specifications, and guidelines.

These clocks can be used as single ended or differential clocks depending upon programmable selection. The ECP3 device also allows internal termination, if needed, to be configured via the Lattice ispLEVER® design software.

Signal	Edge connector pin	FPGA pin	FPGA bank	FPGA function
B3CKN	38	U19	3	Negative bank 3 clock
B3CKP	36	U20	3	Positive bank 3 clock
B6CKN	94	N6	6	Negative bank 6 clock
B6CKP	92	N5	6	Positive bank 6 clock

Table 5: External user clock connections

2.e External I/O Group

A 32 signal wide I/O group with flexible configuration is available on the HV3 module's external connector. This group consists of:

- A large number of I/O pins: 40

- An optional configurable power supply voltage

- Optional reference V_{Ref} and termination V_T voltages

The power supply connects to the VCCIO of banks 3 and 6. There are 2 ways to use it:

- By default, VCCIO is 3.3V. VIO is shorted to 3.3V and the connector power pins are unused.

- Optionally, the connector power pins are used for a different supply voltage VIO such as 1.2V, 1.5V, 1.8V, or 2.5V. In this case the configuration strap VIO must be cut or removed. Refer to illustration 5 for clarification.

- Banks 3 and 6 can be configured independently.

The optional reference voltage is used for externally referenced standards such as H/SSTL.

These options give the designer the ability to easily interface with other devices using advanced system I/O standards. Refer to the Lattice technical notes describing the sysIO standards available and implementation rules using the Lattice ispLEVER® design software.

Signal	Edge connector pin	FPGA pin	FPGA bank number
R3IO0	16	AA26	3
B3IO1	18	AB26	3
B3IO2	20	AC26	3
B3IO3	22	AC25	3
B3IO4	24	AE25	3
B3IO5	26	AF24	3
B3IO6	28	AF23	3
B3IO7	30	AE23	3
B3IO8	15	V21	3
B3IO9	17	V22	3
B3IO10	19	AA25	3
B3IO11	21	Y24	3
B3IO12	23	AB24	3
B3IO13	25	AC24	3
B3IO14	27	AD23	3
B3IO15	29	AC23	3
B6IO0	98	AE4	6
B6IO1	100	AF4	6
B6IO2	102	AD1	6
B6IO3	104	AD2	6
B6IO4	106	AA1	6
B6IO5	108	AA2	6
B6IO6	110	V1	6
B6IO7	112	U2	6
B6IO8	97	AC2	6
B6IO9	99	AC3	6
B6IO10	101	AA3	6
B6IO11	103	AA4	6
B6IO12	105	Y3	6
B6IO13	107	W3	6
B6IO14	109	T1	6
B6IO15	111	U1	6
B3REF	10	T20 - U21	3
B6REF	116	P5 - P6	6
VT3	9	P20	3
VT6	115	P7	6
VIO3	11 - 12	P18 – P19 – R19 - U18	3
VIO6	113 - 114	P8 – P9 – R8 - U9	6

Table 6: Connections of IO group



Illustration 5: Optional IO power supply configuration strap

3 INTERNAL I/Os

3.a On Board Oscillator

A low jitter 125MHz oscillator is installed on the module. It directly feeds both a GPLL on pin M3 and a GDLL on pin K3, both on bank 7. The clock trace is terminated with a 400Ω resistor to ground.

The PLL can be used to generate other required frequencies such as the 200MHz clock for the DDR2 memory.

3.b DDR2 Memory

The pair of DDR2 memory circuits on the module are MT47HxxM16BG from Micron, or equivalent, with a standard JEDEC interface. The modules are factory configured with densities ranging from 512Mb to 2Gb. Refer to the “Ordering information” section for verifying the memory density implanted on your module.

The data access is 16 parallel bits per clock edge with a 200MHz maximum clock frequency.

The interface to the FPGA is implemented via banks 0, 1, and 2 which are allocated solely to the DDR2 use. They are therefore powered with 1.8V for compatibility with the SSTL18 standard. Both banks 0 and 1, used for the I/O data bus, have a reference voltage of 0.9V to their VREF1 pins D5 and G18. The VREF signal on the two memory circuits (pin J2) is a 0.9V reference too.

The termination scheme on the differential clock signals (CLK, LDQS, UDQS) is a 100Ω resistor across the differential traces.

The address, data, and control lines may make use of the internal termination included in the DDR2 memory circuit to improve reliability by modulating properly the ODT signal. The value of the internal terminating resistors in the memory circuit can be chosen among 50Ω, 75Ω, or 150Ω. Refer to the Micron spec sheet for further clarification www.micron.com. However, the module has also been tested successfully without activating the internal terminating resistors thereby saving power. Although for a long trace, termination may improve the transmission characteristics, the traces are so short on this module that termination may be bypassed.

DDR2 A signal	FPGA pin	Bank n°	IO type	DDR2 A signal	FPGA pin	Bank n°	IO type
A0	A6	0	SSTL18_II	BA0	A13	0	SSTL18_II
A1	C6	0	SSTL18_II	BA1	B6	0	SSTL18_II
A2	D6	0	SSTL18_II	BA2	B13	0	SSTL18_II
A3	C13	0	SSTL18_II	CS	B7	0	SSTL18_II
A4	A5	0	SSTL18_II	CAS	C7	0	SSTL18_II
A5	F7	0	SSTL18_II	RAS	D8	0	SSTL18_II
A6	B4	0	SSTL18_II	WE	F8	0	SSTL18_II
A7	E13	0	SSTL18_II	CKE	C8	0	SSTL18_II
A8	A4	0	SSTL18_II	ODT	A7	0	SSTL18_II
A9	D13	0	SSTL18_II	LDM	D10	0	SSTL18_II
A10	A14	0	SSTL18_II	UDM	F11	0	SSTL18_II
A11	A3	0	SSTL18_II	UDQS+	D12	0	SSTL18D_II
A12	A15	0	SSTL18_II	UDQS-	C11	0	SSTL18D_II
A13	C4	0	SSTL18_II	LDQS+	G10	0	SSTL18D_II
D0	A8	0	SSTL18_II	LDQS-	G9	0	SSTL18D_II
D1	C10	0	SSTL18_II	CLK+	G7	0	SSTL18D_II
D2	D9	0	SSTL18_II	CLK-	H8	0	SSTL18D_II
D3	F10	0	SSTL18_II				
D4	E10	0	SSTL18_II				
D5	B8	0	SSTL18_II				
D6	H10	0	SSTL18_II				
D7	C9	0	SSTL18_II				
D8	B10	0	SSTL18_II				
D9	B12	0	SSTL18_II				
D10	A9	0	SSTL18_II				
D11	B11	0	SSTL18_II				
D12	E11	0	SSTL18_II				
D13	A10	0	SSTL18_II				
D14	E12	0	SSTL18_II				
D15	A11	0	SSTL18_II				

DDR2 B signal	FPGA pin	Bank n°	IO type	DDR2 B signal	FPGA pin	Bank n°	IO type
A0	H24	2	SSTL18_II	BA0	A22	1	SSTL18_II
A1	J26	2	SSTL18_II	BA1	K23	2	SSTL18_II
A2	L25	2	SSTL18_II	BA2	J23	2	SSTL18_II
A3	G24	2	SSTL18_II	CS	F20	1	SSTL18_II
A4	J24	2	SSTL18_II	CAS	K26	2	SSTL18_II
A5	H25	2	SSTL18_II	RAS	K25	2	SSTL18_II
A6	L26	2	SSTL18_II	WE	B21	1	SSTL18_II
A7	G25	2	SSTL18_II	CKE	C21	1	SSTL18_II
A8	K24	2	SSTL18_II	ODT	H23	2	SSTL18_II
A9	G26	2	SSTL18_II	LDM	B19	1	SSTL18_II
A10	F26	2	SSTL18_II	UDM	B15	1	SSTL18_II
A11	L24	2	SSTL18_II	UDQS+	F13	1	SSTL18D_II
A12	H26	2	SSTL18_II	UDQS-	F14	1	SSTL18D_II
A13	M24	2	SSTL18_II	LDQS+	G14	1	SSTL18D_II
D0	E15	1	SSTL18_II	LDQS-	F15	1	SSTL18D_II
D1	B20	1	SSTL18_II	CLK+	C19	1	SSTL18D_II
D2	E16	1	SSTL18_II	CLK-	D19	1	SSTL18D_II
D3	A21	1	SSTL18_II				
D4	A20	1	SSTL18_II				
D5	C20	1	SSTL18_II				
D6	A19	1	SSTL18_II				
D7	D15	1	SSTL18_II				
D8	C14	1	SSTL18_II				
D9	A17	1	SSTL18_II				
D10	C17	1	SSTL18_II				
D11	A18	1	SSTL18_II				
D12	B17	1	SSTL18_II				
D13	C16	1	SSTL18_II				
D14	B16	1	SSTL18_II				
D15	C15	1	SSTL18_II				

Table 7: DDR2 interface pin out and signal type

3.c CFI Flash Memory

The CFI flash memory circuit on the module is an S29GLxxP from Spansion, or equivalent, with a standard JEDEC interface. The modules are factory configured with densities ranging from 512Mb to 1Gb. Refer to the "Ordering information" section for verifying the memory density implanted on your module.

The data access is configurable to either 8bit or 16bit according to the BYTE signal selection. Refer to the device spec sheet for clarification.

The interface to the FPGA is implemented via bank 7 which are allocated solely to the CFI flash use. They are therefore powered with 3.3V.

The CFI reset signal, RST#, is tied to the board wide power on reset signal.

CFI signal	FPGA PIN	Bank n°	CFI signal	FPGA PIN	Bank n°
A0	L6	7	D0	L3	7
A1	K6	7	D1	K7	7
A2	H6	7	D2	L5	7
A3	G5	7	D3	J7	7
A4	G6	7	D4	L2	7
A5	J6	7	D5	K5	7
A6	H5	7	D6	K2	7
A7	B2	7	D7	J4	7
A8	E4	7	D8	M4	7
A9	D1	7	D9	K8	7
A10	F3	7	D10	K4	7
A11	G2	7	D11	N4	7
A12	E1	7	D12	J5	7
A13	D2	7	D13	L1	7
A14	F1	7	D14	J1	7
A15	G1	7	D15/A-1	K1	7
A16	H1	7	WE#	C2	7
A17	B3	7	OE#	M6	7
A18	D4	7	CE#	M5	7
A19	D3	7	WP#/ACC	C3	7
A20	G3	7	BYTE#	D22	8
A21	F4	7	RY/BY#	C1	7
A22	F3	7			
A23	F2	7			
A24	H2	7			
A25	J3	7			

Table 8: CFI flash memory interface pin out

3.d Serial Number

The module serial number is engraved in hardware and is available for readout by the FPGA. The unique silicon serial number is a Maxim DS2411 circuit. Its interface to the FPGA is via the 1-wire protocol. It is connected to the FPGA pin R22, bank 2, configured for 1.8V.

Refer to the software section regarding sample VHDL code to retrieve the serial number.

3.e Temperature sensor

The board temperature sensor is physically located between the 1.8V linear regulator and the FPGA, for monitoring a warm spot.

The temperature sensor with a temperature dependent output period ($10\mu\text{s}/^\circ\text{K}$; $\text{TS0}=\text{TS1}=\text{GND}$) is a Maxim MAX6576 circuit. It is connected to the FPGA pin P23, bank 2, configured for 1.8V.

Refer to the software section regarding sample VHDL code to read the sensor output.

3.f Test Points

Two user defined tests points for oscilloscope clip on probes, TP1 (pin G20) and TP2 (pin G21), are available on the module. These tests points are directly connected to the FPGA. They both belong to the 3.3V powered bank 8.

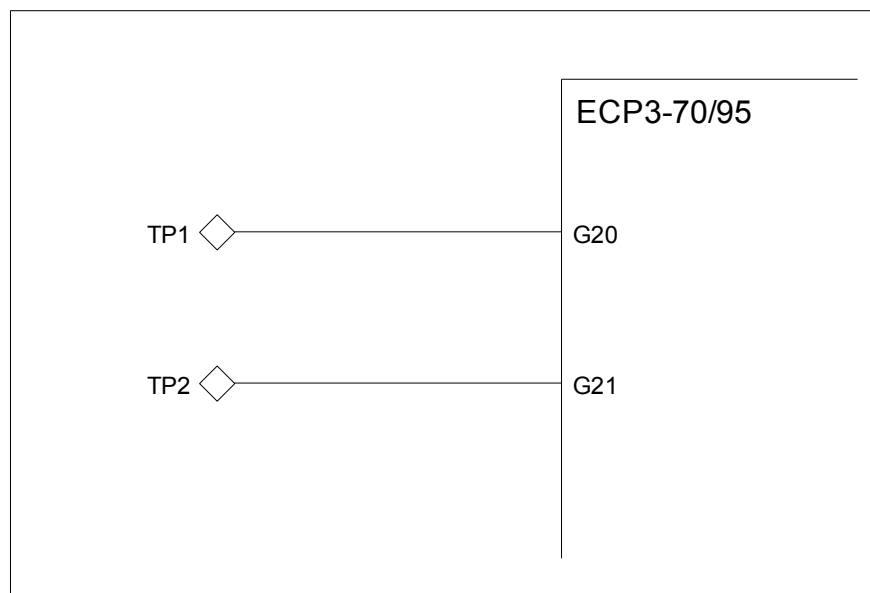


Illustration 6: Test points

3.g Led

A single color surface mount tiny LED for user application is available on the module. It is active low, pulled up on the board through a current limiting 400Ω resistor. It is connected to the FPGA pin E23, bank 8, configured to 3.3V.

Blinking rates or sequences may be programed to indicate various FPGA internal states or variables.

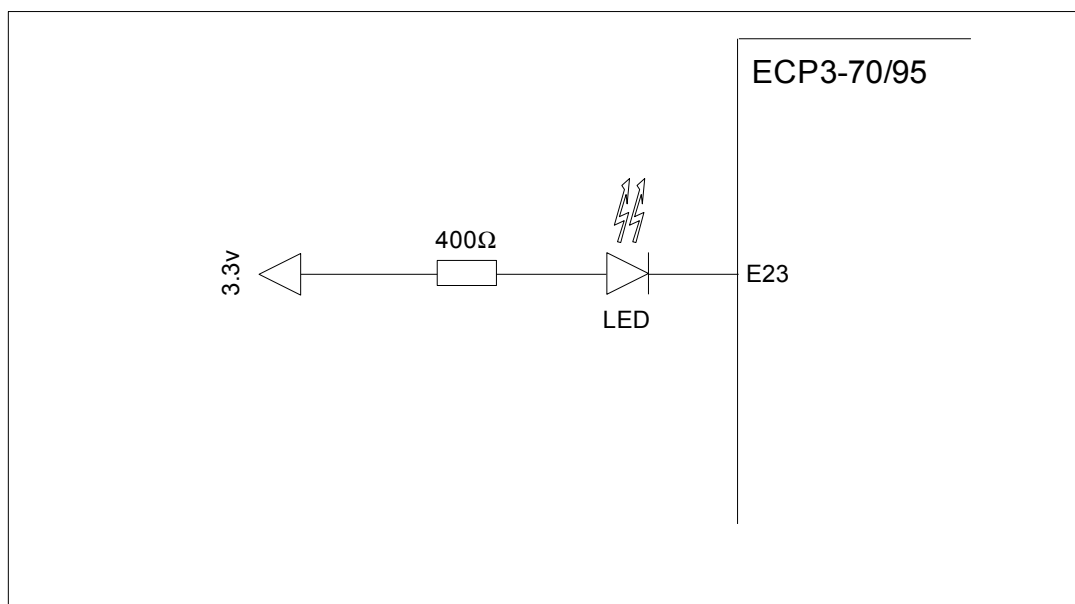


Illustration 7: On board LED

4 CONFIGURATION

4.a JTAG Link

Refer to the Lattice ispDownload Cable reference manual for the JTAG port specification and usage.

Signal	Designation	Edge Connector	FPGA
TDI	Test Data Input	118	F5
TDO	Test Data Output	119	E7
TMS	Test Mode Select	120	E6
TCK	Test Clrok	117	E5

Table 9: JTAG connection

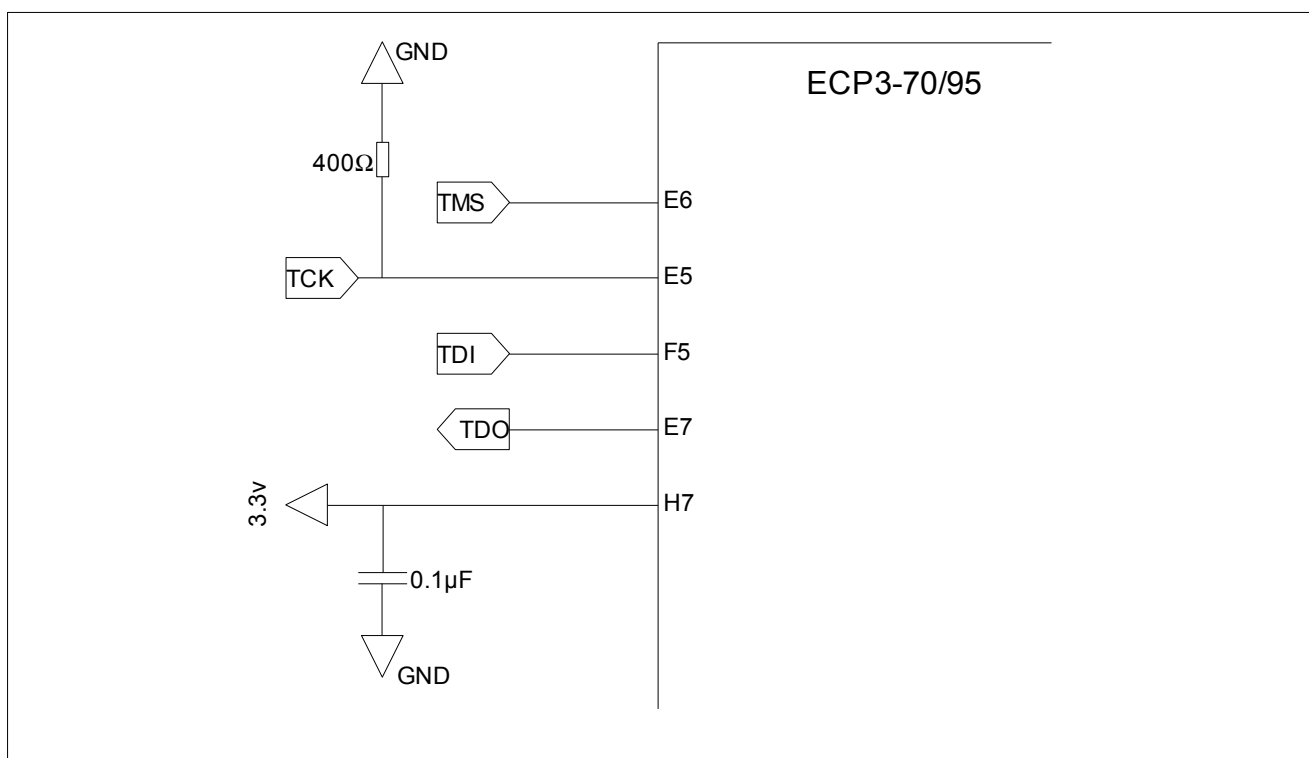


Illustration 8: JTAG connection

4.b FPGA Configuration SPI Flash Memory

The FPGA is automatically configured at power up or after a reset via the on board M25P32 (from STMicro or Numonyx) 32Mb SPI flash. The configuration mode is normal SPI (CFG2:0 to ground, SPIFASTN pulled up).

SPI signal	FPGA pin	Bank number
SPI CS	C24	8
SPI CK	C25	8
SPI DI	K21	8
SPI DO	K20	8

Table 10: Configuration SPI interface

The SPI flash memory can be programmed using the ispVM programming software.

4.c Reset

A reset pin for complete FPGA reboot is provided on the module. This reset forces a fresh reconfiguration of the FPGA with the bit stream stored in the SPI flash. It resets the CFI memory as well.

The reset pin is an active low input with internal pull up to 3.3V. To reset the module, short the pin to ground. If this feature is not used, the pin can be left unconnected and floating.

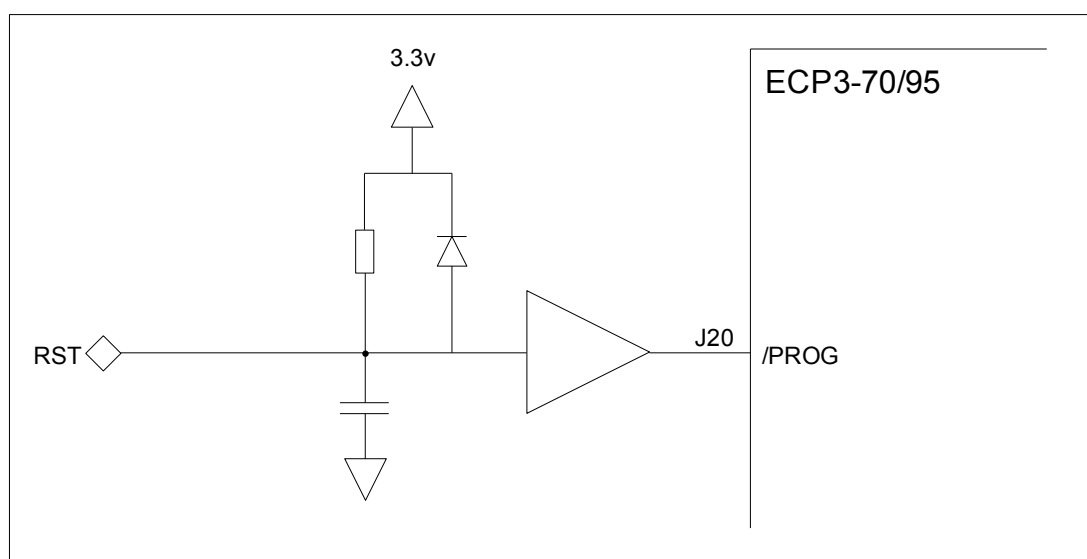


Illustration 9: Reset circuit

5 ORDERING INFORMATION

5.a Module Identification Code

An identification sticker matching the module ordering code is put at the factory on the DDR2 memory circuit. It includes both a module configuration code and a serial number.

The first line is the serial number, which can also be obtained via the FPGA.

The second line shows the precise description of the different components implanted on the module. This is the ordering code.

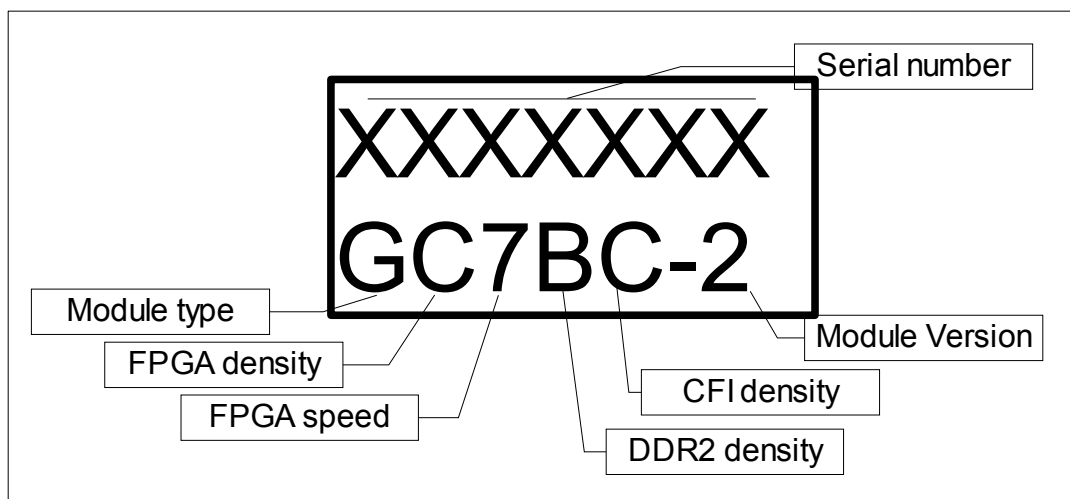


Illustration 10: Module identification sticker

Module type:	HV3 = "G"
FPGA density:	ECP3-70EA = "A", ECP3-95EA = "B", ECP3-150EA = "E", ECP3-70E = "C", ECP3-95E = "D"
FPGA speed:	"6", "7", "8" per Lattice rating -6, -7, -8
DDR2 density:	512Mb = "A", 1Gb = "B", 2Gb = "C"
CFI flash density:	512Mb = "C", 1Gb = "D"

6 SOFTWARE SUPPORT

This module is delivered with an accompanying CD that includes several predefined configuration, constraints, and header files as well as examples projects.

There are also special bit streams for executing specific component tests, such as memory and SERDES.

The software support purpose is to guide and help the designer get going fast and easy in using the module.

Refer to the CD for further explanation.

7 ADDITIONAL INFORMATION

Tachyssema: More information such as design examples, documentation, applications, technical support, board support packages, development & evaluation boards is available from the Tachyssema web site www.tachyssema.com

Lattice: All Lattice spec sheets and user's guides can be downloaded from the Lattice web site www.latticesemi.com

Micron: The DDR2 memory spec sheet and user's guide are available from the Micron web site www.micron.com

Spansion: The CFI flash memory spec sheet and user's guide are available from the Spansion web site www.spansion.com

Maxim: The serial number circuit spec sheet and user's guide are available from the Maxim web site www.maxim-ic.com