

Tachyssema PF120 MODULE PLATFORM User's
Guide

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Preliminary Advanced Information

NOTICES

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Safety informations

While unused and packaged, the platform and associated module must be stored in a proper anti static bag.

Proper grounding technique and anti static methods must be carefully used when the module is inserted in the platform and when external connections to the platform are made.

All power supplies must be off when the module is plugged and external connections are made.

Disclaimer

The information contained in this guide is accurate to the best of our knowledge, but may evolve due to corrections or technical progress without notice.

Package content

Your platform package must contain the following items:

- (1) PF120 platform
- (1) CD with supporting documents, supporting project files, and technical examples

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1 PLATFORM OVERVIEW

1.a Platform Description

The PF120 platform kit is an accompanying accessory to the HV3 module. It can be used for rapid prototyping and development, evaluation, and stand alone embedded and industrial applications.

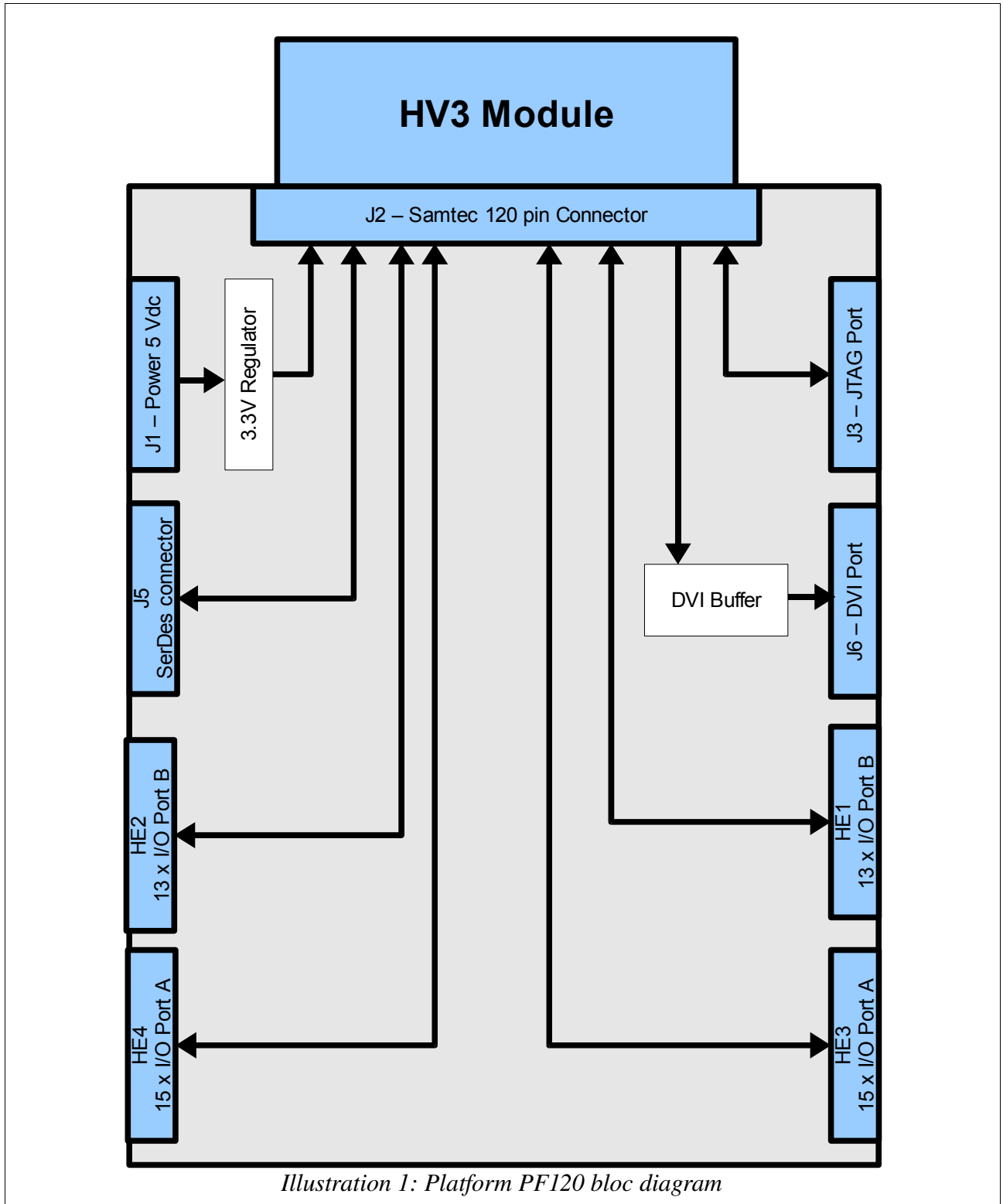
The kit includes all the necessary circuits to directly use the HV3 module as well as several interface connectors for application development. Several extension boards are available for expanding the interface capability of the PF120 system.

The PF120 motherboard kit includes:

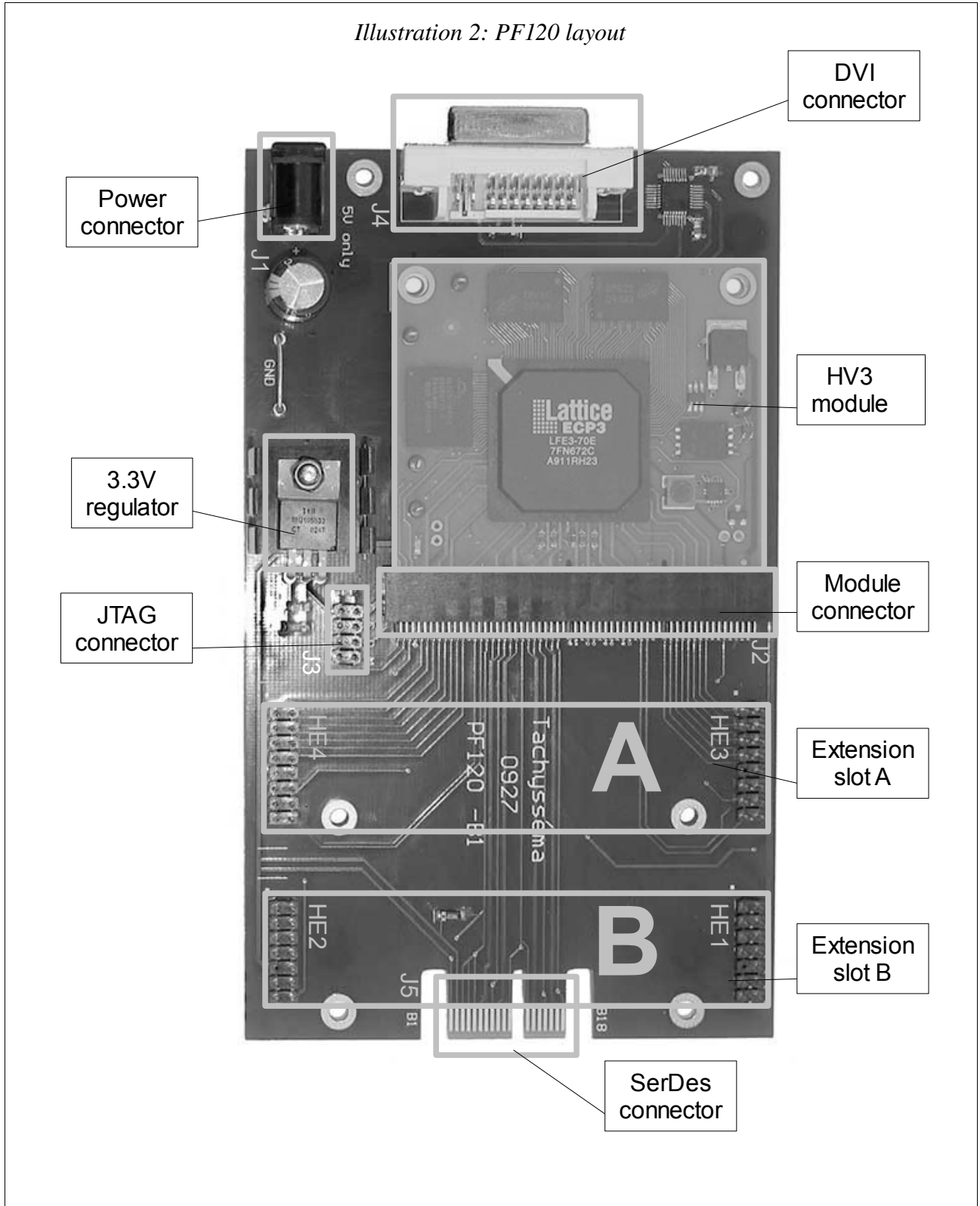
- Regulated 5V external power supply
- On board 3.3V regulator
- DVI output connector
- High speed SerDes interface
- 2,54mm connector array for custom development
- JTAG connector to ispDOWNLOAD Lattice programming cable

The complete schematics for the PF120 platform is available on the accompanying CD.

1.b Bloc Diagram



1.c PF120 Layout



2 DEFINITION OF INTERFACES

2.a PF120 platform board

2.a.1 External Power Supply

The PF120 platform has a connector, J1, for a 5V regulated source. It is recommended to use the provided external power supply.

The connector is a standard 2.1mm ID x 5.5mm OD style with positive center pin.

If using an external power supply other than the provided one, it must be regulated to 5V, otherwise damage may occur to the platform, the plugged-in module, or any plugged external equipment.

2.a.2 JTAG Connector

The J3 connector is dedicated to the JTAG interface. It includes the 4 standard signals as well as the power for running the cable USB or parallel port decoder.

For ease of use, the wires are individually labeled on the ispDOWNLOAD Lattice programming cable with matching letters on the printed circuit.

Cable Signal/Color	JTAG Function	JTAG Connector/Letter
VCC/red	Vcc	1/3
GND/black	Gnd	2/G
TMS/purple	TMS	8/M
TCK/white	TCK	4/C
TDI/orange	TDI	7/I
TDO/brown	TDO	6/O

Table 1: JTAG connector pinout

2.a.3 DVI Interface

The PF120 board includes a DVI output interface without DDC. This interface is brought to an industry standard connector, J4. There is a MAX3814 buffer in line between the FPGA and the connector. The connections are as follows:

DVI signal	J2 pinout (+/-)	FPGA fonction (HV3)
DVICLK	62 / 60	PCS-A3
DVIDAT0	42 / 44	PCS-A0
DVIDAT1	50 / 48	PCS-A1
DVIDAT2	54 / 56	PCS-A2

Table 2: DVI output interface

Note that this DVI interface makes use of the SERDES outputs of the ECP3 FPGA.

2.a.4 SerDes connector

This edge connector (J5, see picture above) is provided for high speed serial expansion. It is connected to the PCS-B of the HV3 FPGA. There are 4 differential input pairs, 4 differential output pairs and 1 differential reference clock pair.

The form factor of this connector is a PCIe x4 without the pinout assignment.

It is capable of carrying the full speed of the ECP3 SerDes.

SerDes Signal	J2 pinout (+/-)	J5 pinout (+/-)
PCS-B CLK	93 / 91	A3 / A4
PCS-B OUT0	68 / 70	B17 / B16
PCS-B OUT1	76 / 74	B13 / B14
PCS-B OUT2	80 / 82	B10 / B9
PCS-B OUT3	88 / 86	B6 / B7
PCS-B IN0	67 / 69	A17 / A16
PCS-B IN1	75 / 73	A13 / A14
PCS-B IN2	79 / 81	A10 / A9
PCS-B IN3	87 / 85	A6 / A7
GND	-	A2-A5-A8-A11-A12-A15-A18-B3-B4-B5-B8-B11-B12-B15-B18
3R3	-	A1-B1-B2

Table 3: SerDes connector pinout

2.a.5 A and B extension slots

These extension slots are provided for generic I/O boards using PIOs. They include power pins, dedicated clock and reference pins.

The 4 headers are designed to be used by pairs, for 2 slots. However they could also be used individually for 4 different extension slots, or a single quad slot. Typically extension slot A uses headers HE3 and HE4; slot B uses headers HE1 and HE2.

The headers are standard HE10, 2.54mm pitch. The 4 headers are spaced by a multiple of 2.54mm, so that a larger connector can fit over 2 board headers.

HE1 and HE2 are keyed 14 pin headers; HE3 and HE4 are keyed 16 pin headers.

Header signal	Header pinout	J2 pinout	FPGA pinout (HV3)
HE1-1	1	15	V21
HE1-2	2	17	V22
HE1-3	3	19	AA25
HE1-4	4	21	Y24
HE1-5	5	23	AB24
HE1-6	6	25	AC24
HE1-7	7	27	AD23
HE1-8	8	29	AC23
HE1-GND	11 - 12		
HE1-3R3	10		
HE1-P5	14		
HE1-KEY	9		
HE2-1	1	111	U1
HE2-2	2	109	T1
HE2-3	3	107	W3
HE2-4	4	105	Y3
HE2-5	5	103	AA4
HE2-6	6	101	AA3
HE2-7	7	99	AC3
HE2-8	8	97	AC2
HE2-GND	11 - 12		
HE2-3R3	10		
HE2-P5	14		
HE2-KEY	9		

Table 4: Expansion slot B pinout

Header signal	Header pinout	J2 pinout	FPGA pinout (HV3)
HE3-1	1	16	AA26
HE3-2	2	18	AB26
HE3-3	3	20	AC26
HE3-4	4	22	AC25
HE3-5	5	24	AE25
HE3-6	6	26	AF24
HE3-7	7	28	AF23
HE3-8	8	30	AE23
HE3-REF	13	10	T20 - U21
HE3-CLK+	16	36	U20
HE3-CLK-	15	38	U19
HE3-GND	11 - 12		
3R3	10		
HE3-P5	14		
HE3-KEY	9		
HE4-1	1	112	U2
HE4-2	2	110	V1
HE4-3	3	108	AA2
HE4-4	4	106	AA1
HE4-5	5	104	AD2
HE4-6	6	102	AD1
HE4-7	7	100	AF4
HE4-8	8	98	AE4
HE4-REF	13	116	P5 - P6
HE4-CLK+	16	92	N5
HE4-CLK-	15	94	N6
HE4-GND	11 - 12		
3R3	10		
HE4-P5	14		
HE4-KEY	9		

Table 5: Expansion slot A pinout

2.b Constraint file

A constraint file with all the pad information from the connectors described above is available on the CD.

2.c Schematics

The PF120 board complete schematics is available on the CD for further reference.

3 SOFTWARE SUPPORT

This platform is delivered with an accompanying CD that includes several predefined configuration, constraints, and header files as well as examples projects.

There are also special bit streams for executing specific component tests, such as memory.

The software support purpose is to guide and help the designer get going fast and easy in using the module.

Refer to the CD for further explanation.

4 ADDITIONAL INFORMATION

Tachyssema: More information such as design examples, documentation, applications, technical support, board support packages, development & evaluation boards is available from the Tachyssema web site www.tachyssema.com

Lattice: All Lattice spec sheets and user's guides can be downloaded from the Lattice web site www.latticesemi.com

Maxim: The DVI driver circuit spec sheet and user's guide are available from the Maxim web site www.maxim-ic.com